

RF Power Field Effect Transistor

HC-DSL09S001N

Document Number: DSL09S001N

Rev. 1, 5/2018

N-Channel Enhancement-Mode MOSFET

Designed for handheld two-way radio applications with frequencies from 136 to 941 MHz. The high gain, ruggedness and Broadband performance of this device make it ideal for large-signal, common-source amplifier applications in handheld radio equipment.

136–941 MHz, 1.0W, 3.7 V BROADBAND RF POWER TRANSISTOR

Typical Broadband EVB Performance ($I_{DQ}=200\text{mA}$, $T_A = 25^\circ\text{C}$, CW)

VDD	Freq.	Pout		Gmax
[V]	[MHz]	[dBm]	[Watts]	[dB]
3.7	400	31.2	1.3	18.9
	440	31.1	1.3	19.1
	460	31.1	1.3	18.5
	480	31.0	1.3	18.2

Typical Narrowband EVB Performance ($I_{DQ}=200\text{mA}$, $T_A = 25^\circ\text{C}$, CW)

VDD	Freq.	Pout		PAE
[V]	[MHz]	[dBm]	[Watts]	[%]
3.7	430	32.1	1.6	53.4
	450	32.7	1.8	57.2
	470	32.6	1.8	62.3

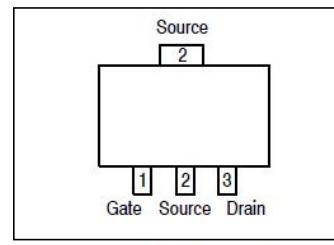
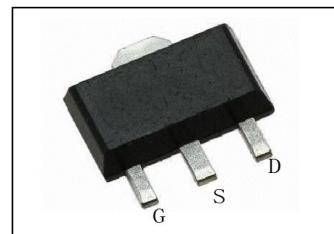


Figure 1. Pin Connections

- Capable of Handling 20:1 VSWR@6.0Vdc, 2.0Watts, CW

Features

- Characterized for Operation from 136 to 941 MHz
- Unmatched Input and Output Allowing Broad Frequency Range Utilization
- Integrated ESD Protection
- Broadband – Full Power Across the Band
- Exceptional Thermal Performance
- Extreme Ruggedness

Typical Applications

- Output Stage VHF Band Handheld Radio
- Output Stage UHF Band Handheld Radio
- Output Stage for 700–800 MHz Handheld Radio
- Driver for 10–1000 MHz Applications

Table1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +20	Vdc
Gate-Source Voltage	V_{GS}	-5.0, +8	Vdc
Operating Voltage	V_{DD}	0, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	-40 to +150	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Power Dissipation @ $T_C=25^\circ\text{C}$	PD	5	W

Table2. ESD Protection Characteristic

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	A, passes 100 V
Charge Device Model (per JESD22-C101)	IV, passes 2000 V

Table3. Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

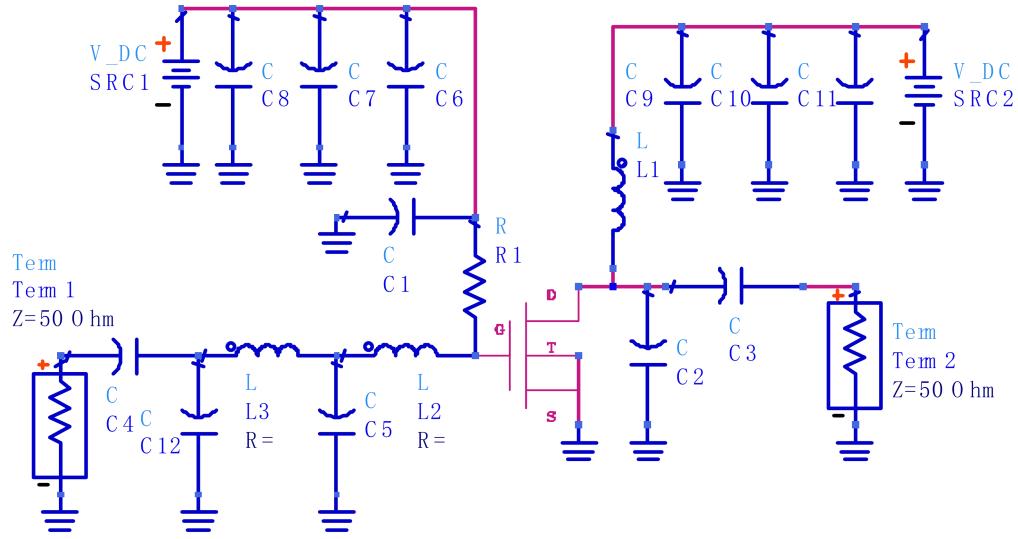
Characteristic	Symbol	Min	Typ.	Max	Unit
Off Characteristics					
Gate-Source Leakage Current	I_{GSS}	-	-	1	uAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS}=16\text{Vdc}$, $V_{GS}=0\text{Vdc}$)	I_{DSS}	-	-	2	µAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS}=3.7\text{Vdc}$, $V_{GS}=0\text{Vdc}$)	I_{DSS}	-	-	1	µAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS}=3.7\text{Vdc}$, $I_D=1\text{mA}$)	$V_{GS(\text{th})}$	1.2	1.5	1.8	Vdc
Gate Quiescent Voltage ($V_{DD}=3.7\text{Vdc}$, $I_D=200\text{mA}$ Measured in Functional Test)	$V_{GS(Q)}$	1.3	2.0	2.7	Vdc
Drain-Source On-Voltage ($V_{GS}=5\text{Vdc}$, $I_D=200\text{mA}$)	$V_{DS(\text{ON})}$	-	0.09	-	Vdc

Dynamic Characteristics

Reverse Transfer Capacitance ($VDG=3.7\text{V}$, Level=30mVac@1MHz)	C_{RSS}	-	2.4	-	pF
Output Capacitance ($VDS=3.7\text{V}$, Level=30mVac@1MHz)	C_{OSS}	-	9.1	-	pF
Input Capacitance ($VGS=5\text{V}$, Level=30mVac@1MHz)	C_{ISS}	-	32.0	-	pF

Typical Performances (In DuSemi Narrowband Test DEMO, 50 Ohm system)Frequency=450MHz, $V_{DS}=3.7\text{Vdc}$, $I_{DQ}=200\text{mA}$, $T_A=25^\circ\text{C}$

Power Gain	G_{PS}	-	19	-	dB
Output Power	P_{out}	-	31	-	dBm
Drain Efficiency	η_D	-	60	-	%

Broad Band Evaluation Circuit (@VDD = 3.7V, f = 440 MHz)

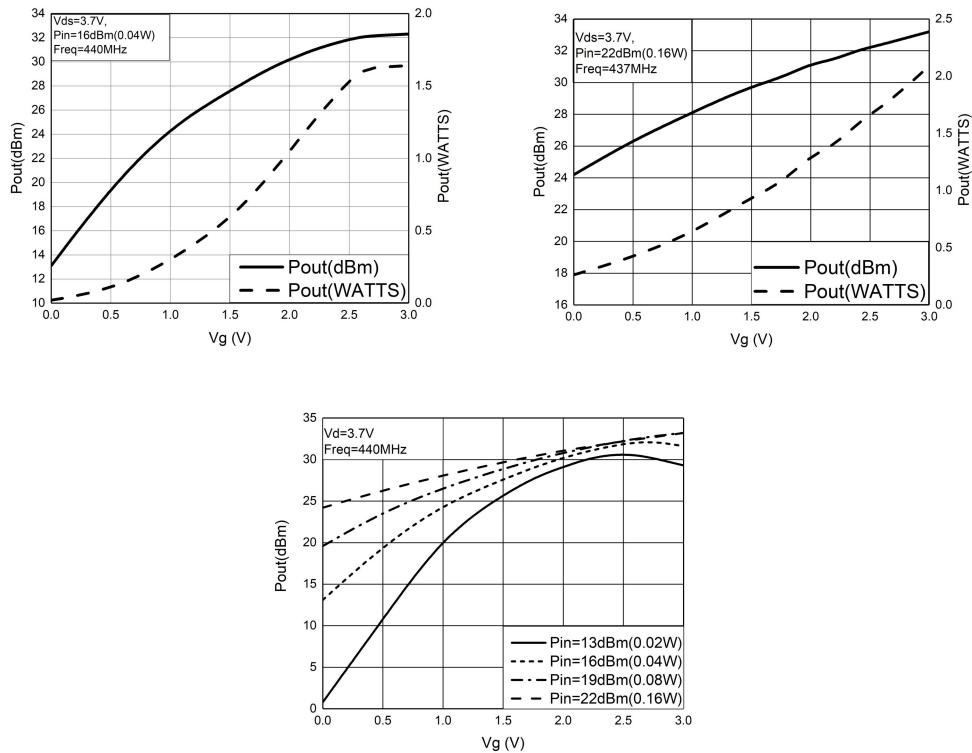
Test Circuit Component Layout

Table4. Test Circuit Component Designations and Value

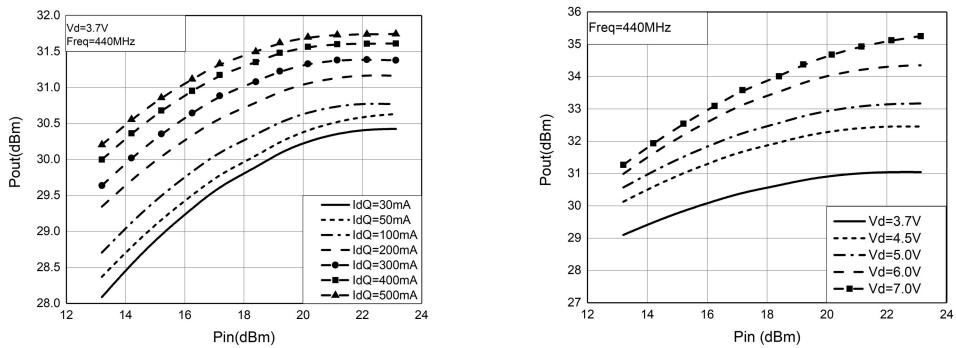
Part	Description	Part Number	Manufacturer
R1	1KOhm	—	—
L2,L3	1nH	—	—
L1	8 Turns D: 0.5 mm, φ 2.4 mm Enamel Wire	—	—
C1, C3,C4,C6,C9	100pF Chip Capacitors	GQM21P5C1H101JB01	Murata
C2, C5	10pF Chip Capacitors	GRM1885C1H201JA01	Murata
C7,C10	1000pF Chip Capacitors	GRM1885C1H102JA01	Murata
C8,C11	10uF,10VChip Capacitors	—	—
C12	18pF Chip Capacitors	—	Murata
PCB	FR-4 ,0.030",ε4.5	—	—

Typical Characteristics

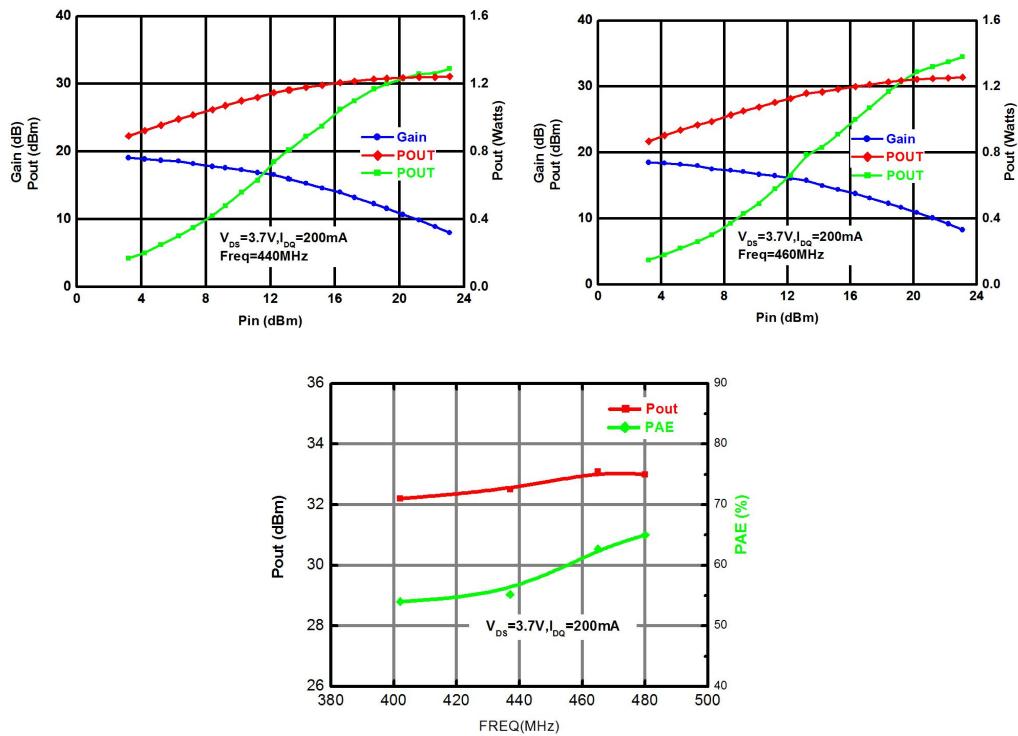
1、440MHz @Vds, Pout VS Vg



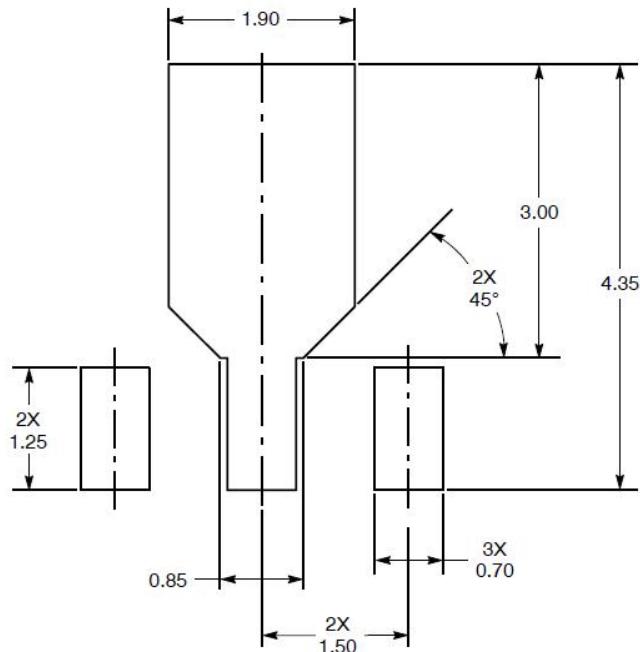
2、440MHz @Vgs, Pout Gain VS Pin



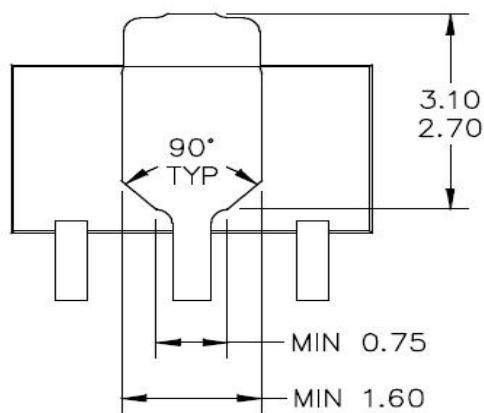
3、Freq@Vds, POUT, Pout Gain VS Pin



Package (Encapsulation)

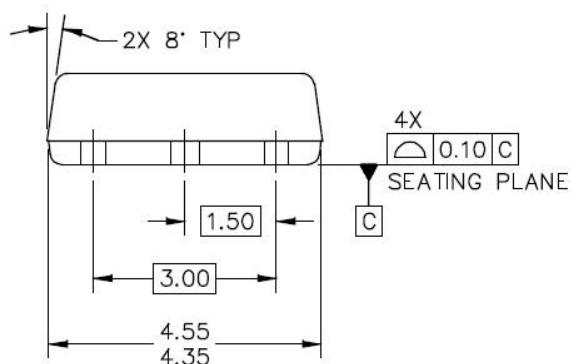
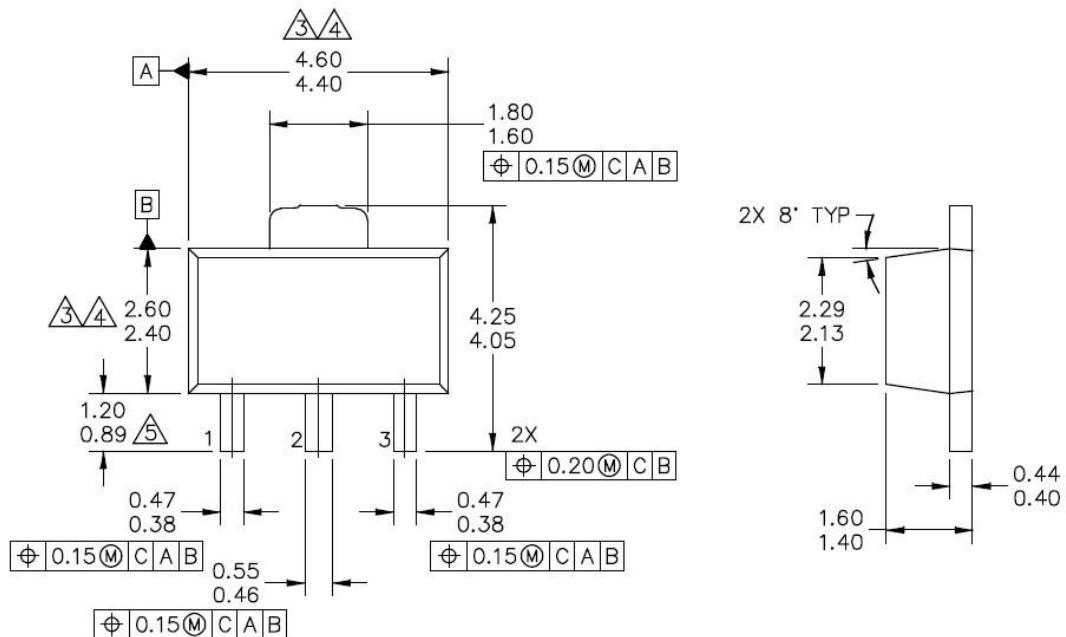


PCB Pad Layout for SOT-89



Bottom View

Package Dimension



REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
1	May 2018	Initial Release of Data Sheet